Description

A SWITCHING POWER SUPPLY DEVICE AND A SEMICONDUCTOR INTEGRATED
CIRCUIT

Technical Field

[0001]

The present invention relates to a switching power source
and a semiconductor integrated circuit and, for example, to
a technique which is effectively applicable to a switching
power source which converts a high voltage into a low voltage
and a semiconductor integrated circuit which is used in the
switching power source.

Background of the invention

[0002]

A switching power source is required to satisfy a low
cost, miniaturization, high efficiency, a low voltage and a
large current.   Accordingly,   as   a   switching   element,   an
N-channel type power MOSFET (hereinafter abbreviated as NMOS)
which is manufactured at a low cost and exhibits the low
ON-resistance (low Ron) and the low Qgd (low gate charge
quantity)   is   used   in   many   cases.   Fig.   12   shows   the
constitution of a step-down type switching power source which
is studied prior to the present invention. In using the NMOS
in a high potential-side switching element M1, a booster
circuit which is referred to as "bootstrap" and a level shifting
circuit shown in the drawing are necessary. In the booster

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circuit shown in Fig. 13, a voltage (VDD-Vf) which is lower than a power source voltage VDD by an amount corresponding to a forward voltage Vf of a diode D4 is supplied for driving high-potential side switching element M1. That is, the voltage which is higher than a source (middle point LX) of the switching element M1 by the voltage (VDD-Vf) stored in the bootstrap CB is supplied to a gate of the switching element M1. To increase the above-mentioned voltage (VDD-Vf), a Schottky barrier diode which exhibits a low forward voltage Vf is used as a diode D4.

[0003]

Fig. 14 shows operational waveforms of respective parts of the step-down-type switching power source shown in Fig. 13. In the step-down-type switching power source, a middle point LX between the high-potential side switching element M1 and the low-potential side switching element M2 is changed to an input voltage Vin and a ground potential VSS for every switching. The booster circuit charges a bootstrap capacity CB from a power source voltage VDD through a diode D4 during a period that a potential of the middle point LX assumes a ground potential VSS. Accordingly, both-end voltages of the bootstrap capacity CB assume the voltage (VDD-Vf) which falls from the power source voltage VDD by an amount corresponding to a forward voltage Vf of the diode D4. When the potential of the middle point LX assumes the input voltage Vin, the diode D4 prevents a

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backward flow to the power source voltage VDD and supplies electricity to a driving circuit of the high-potential side switching element M1 from the bootstrap capacity CB. A driving voltage Vgs of the high-potential side switching element M1 becomes (VDD-Vf).

[0004]

On the other hand, here observed is a tendency that the power source voltage VDD of peripheral circuits including a control circuit is lowered. Accordingly, the lowering of an amount of a forward voltage Vf of the diode D4 is no more ignorable thus giving rise to a possibility that the high-potential side switching element M1 cannot obtain a sufficient driving voltage. When the driving voltage becomes insufficient, the switching element cannot exhibit original performances thereof thus bringing about an increase of loss or the like. Accordingly, an example of a switching power source which constitutes a bootstrap circuit using a junction-type FET (hereinafter abbreviated as JFET) and incorporates an IC therein, there has been known a switching power source disclosed in Japanese Patent Laid-open Hei11(1999)-501500. In this switching power source, the bootstrap capacitor is charged through the JFET.

Patent document 1: Japanese Patent Laid-open Hei11(1999)-501500

Disclosure of the Invention

Problems to be Solved by the Invention

[0005]

However, in the JFET, a leaked current in an OFF state is not ignorable and hence, a diode for preventing a backward flow is connected in series to ensure a sufficiently boosted voltage. That is, to constitute a practical circuit, in the switching power source of the above-mentioned patent document 1, the connection of the backward flow preventing diode is considered necessary thus eventually giving rise to a drawback similar to the drawback which the circuit shown in Fig. 13 possesses.

[0006]

Accordingly, it is an object of the present invention to provide a switching power source which realizes an acquisition of a sufficient driving voltage of a high-potential side switching element M1 even when a power source voltage VDD is low and a semiconductor integrated circuit which is used in the switching power source.

The above-mentioned and other objects and novel features of the present invention will become apparent from the description of this specification and attached drawings.

Means for solving the problems

[0007]

To briefly explain the summary of typical inventions among inventions disclosed in the present application, they

are as follows. That is, in a switching power source which controls a current which flows in an inductor through a switching element which performs a switching operation in response to a PWM (pulse width modulation) signal, and forms an output voltage by a capacitor which is provided in series in the inductor, a booster circuit which is constituted of a bootstrap capacity and a MOSFET is provided between an output node of the switching element and a predetermined voltage terminal, the boosted voltage is used as an operational voltage of a driving circuit of the switching element, and another source/drain region and a substrate gate are connected with each other such that when the MOSFET is made to assume an OFF state, a junction diode between one source/drain region and the substrate gate is inversely directed with respect to the boosted voltage which is formed by the bootstrap capacity.

Advantage of the present invention

[0008]

The switching power source and the semiconductor integrated circuit which use such a switching power source can obtain the sufficient driving voltage of the high-potential-side switching element even when the power source voltage VDD is low.

Best Mode for Carrying out the Invention

[0009]

Fig. 1 shows a schematic circuit of one embodiment of

a switching power source according to the present invention. This embodiment is directed to a so-called step-down-type switching power source which forms an output voltage Vout by stepping down an input voltage Vin. Although not particularly limited, the input voltage Vin may be a relatively high voltage of approximately 12V and the output voltage Vout may be a low voltage of approximately 3V.

[0010]

The above-mentioned input voltage Vin performs the supply of an electric current from one end of an inductor LO through a high-potential side switching element M1. A capacitor CO is provided between another end of the inductor LO and a ground potential VSS of the circuit and the smoothed output voltage Vout is formed by the capacitor CO. Between one end of the inductor LO and the ground potential VSS of the circuit, a switching element M2 which clamps a reverse electromotive voltage which is generated in the inductor LO by allowing a middle point LX to assume the ground potential of the circuit when the switching element M1 assumes an OFF state is provided. The switching elements M1, M2 are formed of an N-channel power MOSFET. A node of the switching elements M1, M2 constitutes the middle point LX of a so-called inverted push-pull output circuit and is connected to one end of the inductor LO.

[0011]

To control the output voltage Vout to a predetermined potential of approximately 3V, a following PWM control circuit is provided. As an example, the above-mentioned output voltage Vout is divided by a voltage dividing circuit which is constituted of resistances R1, R2 and is supplied to one input (-) of an error amplifier EA. A reference voltage Vr is supplied to another input (+) of the error amplifier EA. A differential voltage between the divided voltage and the reference voltage Vr is supplied to one input (-) of a voltage comparator CMP. To another input (+) of the voltage comparator CMP, a triangular wave which is formed by a triangular wave generating circuit TWG is supplied. An output signal of the voltage comparator CMP is supplied to a control circuit CONT and the control circuit CONT forms a PWM signal which makes the divided voltage and the reference voltage Vr coincide with each other. The signal is not particularly limited to the PWM signal and any signal which can control the output voltage Vout by controlling switching of the power MOSFET such as a PFW (pulse frequency modulation) signal, a PDM (pulse density modulation) signal or the like may be used.

[0012]

The control circuit CONT generates a high-voltage-side control signal hg and a low-potential-side control signal lg which correspond to the above-mentioned PWM. In this embodiment, an N-channel-type power MOSFET which exhibits the

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low ON resistance and the low Qgd is used as the above-mentioned switching element M1 thus allowing the control circuit CONT to be operated as a source follower output circuit. Accordingly, to allow the potential of the middle point LX to acquire the high voltage which corresponds to the input voltage Vin, that is, to prevent a phenomenon that the potential of the middle point LX is lowered by an amount corresponding to a threshold value voltage of the MOSFET M1 and a loss is generated, a booster circuit is provided. That is, the booster circuit performs an operation to set the gate voltage when the MOSFET M1 is in an ON state to the high voltage equal to or more than the input voltage Vin by an amount corresponding to the threshold value voltage.

[0013]

The above-mentioned middle point LX is connected to one end of a bootstrap capacity CB. Another end of the bootstrap capacity CB is connected to a power source voltage VDD through a source-drain route of a P-channel-type switching MOSFET M3. The power source voltage VDD is a low voltage such as approximately 5V and is an operational voltage of an error amplifier EA, a voltage comparator CMP and a triangular wave generating circuit TWG which constitute the PWM control circuit including the above-mentioned control circuit CONT, wherein the power source voltage VDD is also used as an operational voltage of low-voltage-side circuits of level

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shifting circuits LS1, LS2 described later.

[0014]

The high-voltage-side control signal hg which corresponds to the above-mentioned PWM signal has a level thereof shifted by the level shifting circuit LS2 thus forming a driving signal HG of the high-voltage-side switching element M1. The level shifting circuit LS2 uses the above-mentioned power source voltage VDD and a boosted voltage Vbt which is formed by the above-mentioned bootstrap capacity CB as operational voltages, wherein by shifting levels of the power source voltage VDD and the high-voltage-side control signal hg having ground potential (approximately 5V in this embodiment) amplitude to the boosted voltage Vbt and a signal having the middle point LX amplitude, it is possible to increase a gate voltage at the time of turning on the switching element M1 to a voltage such as the boosted voltage Vbt.

[0015]

A low-voltage-side control signal lg which corresponds to the PWM signal is basically supplied directly to a gate of a low-potential-side switching element M2 using a buffer or the like. The level shifting circuit LS1 shifts a level of the low-voltage-side control signal lg thus forming a control signal LG which is supplied to a gate of the P-channel-type MOSFET M3. That is, when the low-voltage-side control signal lg of the switching element M2 is inverted by the level shifting

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circuit thus turning off the switch M2, the control signal LG which corresponds to the boosted voltage Vbt is formed and the control signal LG is transmitted to the gate of P-channel-type MOSFET M3 thus turning off the MOSFET M3.

[0016]

The booster circuit of the present invention is characterized by the use of the P-channel-type power MOSFET (abbreviated as PMOS) M3 which constitutes the switching element in place of a diode D4 shown in Fig. 12. Here, the PMOS M3 has a drain terminal D thereof connected to the power source VDD and a source terminal S thereof connected to the bootstrap capacity CB side. The source and the drain of the MOSFET may be reversed depending on the direction in which the voltage is applied and hence, the drain terminal D and the source terminal S shown in the drawing are arranged for a convenience sake. That is, the drain terminal D and the source terminal S imply a drain and a source in a state that the boosted voltage Vbt which is higher than the power source voltage VDD attributed to the bootstrap capacity CB is formed. A substrate gate (a back gate, a channel region or an N-type well region) of the PMOS M3 is connected to the source terminal S-side, that is, the bootstrap capacity CB side.

[0017]

Fig. 2 shows waveforms for explaining an operation of the driving circuit of the switching power source shown in Fig.

1. Basically, during a period in which the switching element M2 is turned on in response to the control signals hg, lg which correspond to the PWM signal (that is, during a period in which the switching element M1 is turned off), the switching element M3 is turned on to charge the bootstrap capacity CB with the power source voltage VDD. In the drawing, this charging voltage is expressed as VDD-V3(on). V3(on) indicates a voltage loss in the source-drain route of the MOSFET M3 during the charging operation and is considered substantially zero.
[0018]

The operation of the PMOS M3 here is referred to as a reverse directional characteristic. That is, the control signal LG of the low level such as a ground potential is supplied to the gate of the PMOS M3 from the level shifting circuit LS1, and the power source voltage VDD side (drain terminal D) is operated as the source region to assume an ON state and hence, charging to the bootstrap capacity CB is started. Here, a charging route is also formed by a parasitic diode which is constituted of a PN junction of the substrate gate and the drain terminal D which is operated as the source and hence, when the potential Vbt on the source terminal S side which is operated as the drain region is lower than (VDD-Vf) (Vf being the forward voltage of the parasitic diode), the charging current also flows through such a parasitic diode.
[0019]

During a period in which the switching element M1 is turned on in response to the control signals hg, lg corresponding to the PWM signal (that is, the switching element M2 is turned on), the potential of the middle point LX is elevated from the low level due to turning-on of the switching element M1. Corresponding to the elevation of the low level, the boosted voltage Vbt of the bootstrap capacity CB is elevated as the voltage which is higher by an amount corresponding to the charging voltage VDD. That is, between the gate and the source (HG-LX) of the switching element M1, a holding voltage VDD (VDD-V3(on)) of the bootstrap capacity CB is applied through the level shifting circuit LS2 and hence, the potential of the middle point LX obtained from the source side is elevated to a high voltage corresponding to the input voltage Vin. Here, VDD is approximately 5V and a threshold value voltage of the switching element M1 is approximately 1V thus establishing the relationship of VDD>Vth.

[0020]

Due to the elevation of the boosted voltage Vbt, to a pair of source, drain of the MOSFET M3, the voltage is applied in the direction opposite to the direction that the voltage is applied to the pair of source and drain regions in the above-mentioned charging operation and hence, as shown in Fig. 1, the boosted voltage Vbt side is operated as the source terminal S and the power source voltage VDD side is operated

as the drain terminal D. Accordingly, assuming that the control signal LG supplied to the gate G is set to a high level such as the power source voltage VDD, when the potential of the source terminal S is elevated to the threshold value voltage Vth or more, the switching element again assumes an ON state and the charge of the bootstrap capacity CB which forms the boosted voltage Vbt is leaked to the power source voltage VDD side. The level shifting circuit LS1 sets the high level of the control signal LG to a high voltage corresponding to the boosted voltage Vbt and maintains an OFF state by setting the gate G and the source terminal S at the same potential (equal to or below Vth). Further, the voltage is applied to the parasitic diode in the reverse direction and no current which discharges the charge of the bootstrap capacity CB flows.

[0021]

The charge of the bootstrap capacity CB which is consumed in one charging operation for bringing the switching element M1 into an ON state can be roughly calculated by Cg×Vgs. Here, symbol Cg indicates a gate input capacity of the switching element M1, and symbol Vgs indicates a driving voltage between the gate and the source. By multiplying the charge with a switching frequency, it is possible to obtain an average charging current. As an example, to calculate the charging current by setting Cg, Vgs and switching frequency as Cg=3000pF and Vgs=5V and the switching frequency = 1MHz, the charging

current becomes 15mA. Further, the ON resistance of the MOSFET M3 is several tens mΩ in general and hence, the voltage drop V3(on) at the time of charging is small and is regarded as zero. Accordingly, this embodiment can suppress the voltage drop to an extremely small value compared to the voltage drop attributed to the forward voltage Vf of the conventional diode D4.

[0022]

During the period in which the switching element M2 is turned off (during the period in whihc the switching element M1 is turned on) as described above, it is necessary to turn off the P-channel MOSFET M3. To turn off the P-channel MOSFET M3, the level shifting circuit LS1, by using the boosted voltage Vbt as an operational voltage, shifts a level of the control signal LG which is supplied to the gate terminal G of the P-channel MOSFET M3 to a voltage level equal to a voltage level of the boosted voltage Vbt of the source terminal S. Further, there exists a diode which is parasitic between the drain terminal D of the MOSFET M3 and the substrate gate (also referred to as a body diode). Due to this parasitic diode, the MOSFET M3 is brought into the above-mentioned OFF state and, at the same time, a backward flow toward the power sourced voltage VDD from the boosted potential Vbt can be prevented. Accordingly, it is unnecessary to newly provide a diode for preventing a backward flow which the above-mentioned patent

document 1 uses as the JFET.

[0023]

Since transition times to an ON state or an OFF state of the switching elements M1, M2, M3, possess irregularities attributed to the elements or the like, a dead time is provided in the changeover of the switching elements M1, M2 for preventing a through current. In the same manner, when the switching element M3 is turned on before the switching element M1 is completely turned off, a backward flow toward the power source VDD from the boosted potential side is generated and hence, the dead time is provided in the same manner. Although not particularly limited, the dead time is set by the control circuit CONT which forms a signals lg and hg corresponding to the PWM signal. As described above, the present invention provides the booster circuit which can acquire the sufficient driving voltage of the switching element M1 even when the power source voltage VDD is set to the low voltage.

[0024]

Fig. 3 shows a schematic cross-section of an element showing one embodiment of a P-channel MOSFET M3 shown in Fig. 1. Fig. 3(A) shows an example of a general P-channel MOSFET and Fig. 3(B) shows an example of a high-dielectric-strength MOSFET. From the waveforms of signals of respective portions in Fig. 2, it is understood that the boosted voltage Vbt reaches the power source voltage VDD + the input voltage Vin.

Accordingly, as the P-channel MOSFET M3, it is desirable to use an LDMOS (Laterally Diffused MOS) having a high dielectric strength shown in Fig. 3(B) for a safety purpose.

[0025]

In the general P-channel type MOSFET shown in Fig. 3(A), an N-type well region NWEL is formed on a P-type substrate PSUB, and a pair of P+ type source/drain regions are formed in the N-type well region NWEL. On a well region between such a pair of source, drain regions (a channel or a substrate gate), a gate insulation film having a small film thickness is formed. On the gate insulation film, a gate electrode is formed in a state that the gate electrode strides over the pair of source and drain regions. Further, when the P-channel type MOSFET is used as the switching element M3 which constitutes the above-mentioned booster circuit, the well region NWEL and a P+ region which constitutes the source terminal S side in Fig. 1 are connected with each other. Between the P+ region which constitutes the drain terminal D in Fig. 1 and the substrate gate (NWEL), a parasitic diode illustrated in the drawing exists.

[0026]

In the high-dielectric-strength MOSFET shown in Fig. 3(B), a P+ region which constitutes the drain terminal D is formed on a P-type substrate PSUB (P-). With respect to a semiconductor region which corresponds to the source terminal

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S, a P+ region is formed in an N-type well region NWEL in a state that the P+ region faces the P+ region which constitutes the drain terminal D in an opposed manner, and an N+ region for obtaining an ohmic contact is formed in the N-type well region NWEL. Further, by forming electrodes on the P+ region and the N+ region, the connection with the N-type well region NWEL is established. In this high-dielectric-strength MOSFET, with respect to the drain region, the P+ region and the P-substrate are operated as effective drain regions, while a well region (channel or substrate gate) between the P+ regions formed in the N-type well region NWEL is used as the effective substrate gate (channel region).

[0027]

Above the N well region NWEL between the pair of P+ regions and the substrate PSUB, a gate insulation film having a small film thickness is formed. On the gate insulation film, a gate electrode is formed in a state that the gate electrode strides over the pair of P+ regions. Further, when the high-dielectric-strength MOSFET is used as the switching element M3 which constitutes the above-mentioned booster circuit, the well region NWEL and a P+ region which constitutes the source terminal S side in Fig. 1 are connected with each other. Between the substrate PSUB which constitutes a portion of the drain region shown in Fig. 1 and the substrate gate (NWEL), a parasitic diode illustrated in the drawing exists. In such

a LDMOS, the structure of the source region and the drain region is asymmetrical and hence, the source and the drain are expressed as illustrated in the drawing to show this asymmetry.

[0028]

As shown in Fig. 3(A), (B) which are schematic cross-sectional structural views of elements, the MOSFET is used in a state that the source and the substrate gate (well region) are connected with each other and hence, in both of the general P-channel MOSFET shown in Fig. 3(A) and the LDMOS shown in Fig. 3(B), the parasitic diode is present between the drain and the source. Accordingly, there arises no problem in using the P-channel MOSFET and the LDMOS in the switching element M3 in the present invention. Further, in charging the charge to the bootstrap capacity CB of the LDMOS shown in Fig. 3(B), a current is made to flow form the drain to the source in Fig. 3(B). However, this operation is an operation which is performed in a linear region (low current) and hence, there is no possibility that the performance of the switching element M3 is largely lowered.

[0029]

According to the switching power source of this embodiment, even when the power source voltage VDD is lowered, the high-potential-side switching element can obtain the sufficient driving voltage. Since the N-channel power MOSFET can be used in the high-potential-side switching element, it

is possible to constitute an inexpensive and miniaturized switching power source. Further, the switching power source of this embodiment also has an advantage that the switching element can be incorporated into an IC as described later. By incorporating the switching power source into the IC, it is possible to reduce the number of externally mounting parts thus contributing to the miniaturization and the reduction of cost of the power source.

[0030]

In the booster circuit of the present invention, the bootstrap capacity CB is charged by turning on the P-channel MOSFET M3, and the prevention of the backward flow from the boosted potential side is achieved by turning off the MOSFET by shifting the level of the gate voltage of the MOSFET corresponding to the boosted voltage, and by making use of the body diode. Accordingly, it is possible to eliminate the diode for preventing the backward flow which is necessary in the switching power source described in the above-mentioned patent document 1. Further, since the ON resistance of the MOS is small, that is several tens of mΩ, compared to the forward voltage Vf of the diode, it is possible to suppress the lowering of the voltage during the charging. Provided that the sufficient charging time can be set, it is possible to increase the bootstrap capacity CB to VDD.

[0031]

As described above, even when the power source voltage VDD is low, it is possible to obtain the sufficient driving voltage of the high-potential-side switching element M1. Accordingly, this embodiment can adopt the N-channel power MOSFET which can be manufactured at a low cost, can be miniaturized, and can exhibit the low Ron and the low Qgd as the high-potential-side switching element and hence, it is possible to constitute the switching power source which can be manufactured at a low cost and can be miniaturized. Further, since the MOSFET exhibits the smaller chip area compared to the Shottky barrier diode, the MOSFET can be easily incorporated into the IC. Accordingly, it is possible to eliminate an externally mounted diode whereby this embodiment is suitable for the miniaturization and the reduction of cost of the power source.

[0032]

Fig. 4 shows the constitution of one embodiment of the switching power source according to the present invention. In the switching power source of this embodiment, a portion surrounded by a frame indicated by a bold line is constituted of a semiconductor integrated circuit (IC). That is, the high-potential-side switching element M1 and the low-potential-side switching element M2 are constituted of an externally mounted unit element. Further, the inductor LO, the bootstrap capacity CB and the capacitor CO, and the

resistances R1, R2 which constitute the voltage dividing circuit are also constituted of a unit element. In this embodiment, the switching element M3 which constitutes the booster circuit is formed in a state that the switching element M3 is incorporated in the semiconductor integrated circuit. That is, in the semiconductor integrated circuit, besides the MOSFET M3, the error amplifier EA, the voltage comparator CMP, the triangular wave generating circuit TWG, the control circuit CONT, the level shifting circuits LS1, LS2 and the like are formed. Although not shown in the drawing, the driving circuits which drive the MOSFETs M1, M2 are also incorporated in the semiconductor integrated circuit. In this embodiment, by forming control parts into the semiconductor integrated circuit and by incorporating the bootstrap switching element M3 in the semiconductor integrated circuit, it is possible to realize the reduction of number of parts and the miniaturization of the power source.

[0033]

Fig. 5 shows the constitution of another embodiment of the switching power source according to the present invention. Also in this drawing, a portion which is surrounded by a frame indicated by a bold line is constituted of a semiconductor integrated circuit (IC) in the same manner as the above-mentioned embodiment. In this embodiment, by also incorporating the switching elements M1, M2 in the

semiconductor integrated circuit, the number of externally mounting parts can be further reduced and hence, this embodiment is suitable for the miniaturization and the reduction of the cost of the power source.

[0034]

Fig. 6 shows the constitution of still another embodiment of the switching power source according to the present invention. Also in this drawing, a portion which is surrounded by a frame indicated by a bold line is constituted of a semiconductor integrated circuit (IC) in the same manner as the above-mentioned embodiment. In this embodiment, two semiconductor integrated circuits for a control IC and a driver IC are used. The control IC mounts an error amplifier EA, a voltage comparator CMP, a triangular wave generating circuit TWG and a control circuit CONT which constitute a PWM control part thereon and outputs a PWM signal. The driver IC includes switching elements M1, M2, level shifting circuits LS1, LS2, a MOSFET M3 which constitutes a booster circuit, and an inverter circuit INV1 which forms a control signal LG' on a lower potential side upon receiving a PWM signal. In this embodiment, the level shifting circuit LS1 forms a control signal LG of the switching MOSFET M3 upon receiving the PWM signal.

[0035]

Fig. 7 shows the schematic circuit of another embodiment of the switching power source according to the present

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invention. This embodiment is a modification of the embodiment shown in Fig. 1, wherein a diode D1 is used in place of the switching MOSFET M2 on the low voltage side. When the diode D1 is used in this manner, although a voltage loss is generated by an amount corresponding to a forward voltage Vf in an ON state, an ON/OFF is automatically operated due to a potential relationship between an anode and a cathode and hence, the above-mentioned control signal lg becomes unnecessary. In the so-called step-down-type switching power source, the above-mentioned control signals lg, hg have the complementary relationship as shown in Fig. 2. A control signal LG of a MOSFET M3 of a booster circuit of this embodiment may be generated based on the control signal hg of the MOSFET TM1. This embodiment also can adopt the constitutions shown in Fig. 4, Fig. 5 and Fig. 6.

[0036]

Fig. 8 shows the constitution of still another embodiment of the switching power source according to the present invention. Also in this drawing, two semiconductor integrated circuits for a control IC and a driver IC are used in the same manner as the embodiment shown in Fig. 6. A common operational voltage VCC is applied to the control IC and the driver IC, for example. The voltage VCC may be a low voltage such as the above-mentioned VDD or a high voltage corresponding to an input voltage Vin. Accordingly, the driver IC includes a step-down

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power source circuit Reg and forms an internal voltage corresponding to the VDD. On the other hand, the control IC forms the PWM signal corresponding to the above-mentioned power source voltage VCC. Accordingly, the driver IC includes a voltage clamping circuit VCL which receives the PWM signal. Other constitution is substantially equal to the constitution of the embodiment shown in Fig. 6 and hence, their explanation is omitted.

[0037]

In this embodiment, the driver IC requires no particular power source VDD and can use the input voltage Vin as the power source voltage VCC. By stepping down such a high voltage in the inside of the driver IC and by using the stepped-down voltage as the low voltage, it is possible to reduce the power consumption in the internal driver circuit. In this case, the PWM control IC and driver IC are operated with operational voltages different from each other. That is, the control IC is operated with 12V and the driver IC is operated with the internal voltage of 5V and hence, a suitable voltage clamping mean is provided to an input circuit (VCL) of the PWM signal.

[0038]

Fig. 9 shows a circuit of one embodiment of a voltage clamping circuit VCL shown in Fig. 8. The voltage clamping circuit VCL shown in the drawing clamps a level of an input signal (PWM) having high signal amplitude VCC which is supplied

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from an external terminal of the driver IC to a level which
corresponds to an operational voltage VDD level on a low voltage
side of an inverter circuit INV 1 and level shifting circuits
LS1, LS2 of the driver IC.

[0039]

In the input terminal PWM, diodes D2, D3 which constitute
an electrostatic breakdown preventing circuit are provided.
Although not particularly limited, the driver IC of this
embodiment includes two operational voltages, that is, a high
voltage VCC and a low internal voltage VDD which is formed by
a power source circuit Reg. The diode D2 is provided between
the input terminal PWM and the power source terminal VCC, while
the diode D3 is provided between the input terminal PWM and
a ground potential VSS of the circuit. Although not
particularly limited, the power source voltage VCC is a high
voltage of approximately 12V and the internal voltage VDD is
a low voltage of approximately 5V.

[0040]

The input terminal PWM is connected to one source-drain
route of the N-channel MOSFET M4 which constitutes the voltage
clamping circuit. The internal voltage VDD is supplied to a
gate of the MOSFET M4 as a voltage to be restricted. An output
voltage which is clamped by the internal voltage VDD is obtained
from another source-drain route of the MOSFET M4 and is
transmitted to an input terminal of an input circuit IB. In

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this embodiment, to perform the voltage clamping operation by the MOSFET M4 in a stable manner, a current source Io is provided between another source-drain route and a ground potential of the circuit. Further, a capacitor Ci is provided in parallel to the current source Io.

[0041]

In this embodiment, an input signal having large signal amplitude such as VCC-0V (12V-0V) indicated as a waveform in the drawing is supplied to the input terminal PWM, while from another source-drain route of the MOSFET M4, a voltage whose signal amplitude is shifted to the small restricted value by the power source VDD such as (VDD-Vth)-0V is outputted. Further, an output voltage Vo which passes the input circuit IB has CMOS amplitude such as VDD-0V (5V-0V) as indicated by a waveform in the drawing. Here, Vth is a threshold value voltage of the MOSFET M4. Although not particularly limited, the MOSFET M4 is formed on the P-type well region which is electrically separated from the substrate and such a P-type well (channel region) is connected to another source-drain route which constitutes an output side of the MOSFET M4.

[0042]

In the above-mentioned voltage clamping circuit, when a leak current route attributed to a high resistance generated by the defective insulation of the circuit or the like is formed at a node V on an output side of the MOSFET M4, the potential

is elevated and hence, the MOSFET M4 is held in an OFF state whereby, unless the above-mentioned current source Io is present, the voltage clamping operation becomes inoperable. By providing the current source Io, the elevation of the potential on the output node side can be suppressed and hence, the stable voltage clamping operation can be performed. Accordingly, it is sufficient to set the current source Io to a fine current which is larger than a leaked current and is not regarded as defective thus realizing the low power consumption.

[0043]

Further, a parasitic capacity Cds is present between the source and the drain of the MOSFET M4. Due to this parasitic capacity Cds, when the input signal PWM is changed to a high voltage such as VCC, there arises a drawback that the voltage on the output side is changed to a level equal to or more than the power source voltage VDD due to coupling. To obviate such a drawback, the capacitor Ci is provided in parallel to the current source Io. Due to such a constitution, the parasitic capacity Cds and the capacitor Ci are connected in series and the input voltage PWM is divided corresponding to an inverse proportion of a capacity ratio thus preventing the output side node from having the voltage level equal to or more than the power source voltage VDD.

[0044]

Here, although a gate capacity of the MOSFET which constitutes an input circuit is present in the input circuit IB, only with such a gate capacity, the voltage of the output side node is changed to a level equal to or more than the power source voltage VDD due to the above-mentioned coupling. Accordingly, the capacitor Ci is set to a value which is sufficiently large compared to the input capacity of the input circuit IB. In this embodiment, although the voltage clamping circuit is applied to the input signal PWM, this circuit is applicable to the input signal of a voltage level higher than the internal operational voltage. As an example, an operational ON/OFF control signal of the driver IC or the like may be named. By applying the clamping circuit shown in Fig. 9 to the terminal to which the input signal PWM shown in Fig. 8 is inputted, this embodiment can respond to the high-speed change of the PWM signal thus realizing an accurate control of the driver IC.

[0045]

Fig. 10 shows a circuit of one embodiment of the level shifting circuit LS2 which is used in the switching power source according to the present invention. In the level shifting circuit of this embodiment, a CMOS inverter circuit INV2 which is operated with a power source voltage VDD is provided as an input circuit. As an input of the inverter circuit INV2, the control signal hg is supplied. An output signal of the

inverter circuit INV2 is supplied to a gate of an N-channel MOSFET M5. A load resistance R3 is provided between a drain of the MOSFET M5 and a boosted voltage Vbt. Although not specifically limited, a resistance R4 is provided between the source of MOSFET M5 and a ground potential of a circuit. The drain output of the above-mentioned MOSFET M5 is outputted as a driving signal HG which has a level thereof shifted through CMOS inverter circuits INV3 and INV4 which are operated with the boosted voltage Vbt and a potential of the middle point LX.

[0046]

When the control signal hg is at a low level (VSS), the output signal of the inverter circuit INV2 assumes a high level so as to bring the MOSFET M5 into an ON-state. An operating point of the circuit in this state can be obtained as follows. In Fig. 10, assuming a gate voltage of MOSFET M5 as Vi, a source voltage as Vs, a drain voltage as Vo, a gate-source voltage as Vgs, a current which flows through the resistance R4 as Is and a current which flows through the resistance R3 as Id, following relationships are established.

[0047]

$$Vs = Vi - Vgs = Is \times R4 \qquad \ldots \text{Formula (1)}$$

$$Is \cong Id \qquad \ldots \text{Formula (2)}$$

$$Vo = Vbt - Id \times R3 \cong Vbt - Is \times R3 \ldots \text{Formula (3)}$$

In the formula (1), Vgs is a value which is determined

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based on the characteristic of the above-mentioned MOSFET M5.

The following relationship is derived from above-mentioned formulae.

$$Vo=Vbt-(Vi-Vgs) \times (R3/R4) \quad \quad ....(4)$$

Here, values of the above-mentioned resistances R3, R4 are determined so as to set an input voltage of the inverter circuit INV3, that is, the above-mentioned drain voltage Vo to a potential lower than a logic threshold value of the drain voltage Vo. Accordingly, the inverter circuit INV3 outputs a high level corresponding to the boosted voltage Vbt, and a low-level driving signal HG corresponding to the potential of the middle point LX is formed by the inverter circuit INV4.
[0048]

When the control signal hg assumes a high level (VDD), the output signal of the inverter circuit INV2 assumes a low level so as to bring the MOSFET M5 into an OFF-state. Accordingly, the drain output of the MOSFET M5 is outputted as a high-level voltage such as the boosted voltage Vbt due to the resistance R3. Accordingly, the input voltage of the inverter circuit INV3 assumes a potential higher than a logic threshold value of the input voltage and outputs a low level corresponding to the potential of the middle point LX, while a high-level driving signal HG corresponding to the boosted voltage Vbt is formed by the inverter circuit INV4. The above-mentioned level shifting circuit is characterized in

that the output of the circuit is fixed even at the time of supplying the power source and does not fall into an unstable state which a conventional latch-type level shifting circuit falls.

[0049]

The level shifting circuit LS1 which forms a control signal LG to be supplied to the gate of the switch of MOSFET M3 is also constituted of a substantially equal circuit as indicated by a parenthesis in Fig. 10. Here, a low potential side of the inverter circuits INV3, INV4 assumes the ground potential (VSS) of the circuit. When an inverting signal of a control signal (lg) is outputted as the control signal (LG), the above-mentioned inverter circuit INV4 is omitted.

[0050]

Fig. 11 shows a schematic circuit diagram of another embodiment of the switching power source according to the present invention. This embodiment is a modification of the embodiment shown in Fig. 1, wherein an N-channel MOSFET M3' is used as a switching element of the booster circuit. In using the N-channel MOSFET M3' in this manner, to turn on the MOSFET M3 for charging the bootstrap capacity CB up to the power source voltage VDD, it is necessary to set the gate voltage to the power source voltage VDD or more. For this end, the level shifting circuit LSI is operated based on the boosted voltage VCC. This VCC may be supplied from the outside, or may be formed

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of the similar booster circuit. In this manner, when the N-channel MOSFET is used, the source, drain regions of the power source voltage VDD side and the substrate gate are connected with each other, and a parasitic diode between the source and drain regions on the boosted voltage side and the substrate gate is utilized for preventing the backward flow. Since the circuit for generating the boosted voltage VCC becomes necessary, the P-channel MOSFET is superior to the N-channel MOSFET as the switching element of the booster circuit.

[0051]

Fig. 12 shows the constitution of still another embodiment of the switching power source according to the present invention. This embodiment is a modification of the embodiment shown in Fig. 6. Although the driver IC may be constituted of the semiconductor integrated circuit which is formed on one semiconductor substrate as shown in Fig. 6, in this embodiment, the above-mentioned MOSFETs M1, M2 and other circuits are respectively prepared using processes suitable for respective circuits on semiconductor chips (semiconductor substrates) Chip 1, Chip 2, Chip 3 which are indicated by a chain line in Fig. 12, and these parts are sealed in one package as the multiple chip module constitution thus forming a semiconductor integrated circuit device. Further, three semiconductor integrated circuit devices may be constituted by sealing the respective semiconductor chips Chip 1, Chip 2,

Chip 3 in separate packages and a circuit may be constituted by connecting these semiconductor integrated circuit devices with each other on a mounting substrate.

[0052]

Although the invention which is made by inventors of the present invention has been specifically explained in conjunction with the embodiments, the present invention is not limited to such embodiments and various modifications can be made without departing from the gist of the present invention. For example, the switching element M2 on the low potential side may be provided with a driving circuit which is driven with a high voltage. In this case, it is possible to clamp a middle point LX which is generated in the inductor to a ground potential by a small ON resistance value of the switching element M2 and hence, the switching element can be further miniaturized or is further efficiently operated. Specific circuits of the level shifting circuit LS1, LS2 may adopt various modes for carrying out the invention. The present invention is broadly applicable to switching power source devices.

Brief Explanation of Drawings

[0053]

Fig. 1 is a schematic circuit diagram showing one embodiment of a switching power source according to the present invention.

Fig. 2 is a waveform diagram for explaining an operation of a driving circuit of the switching power source shown in Fig. 1.

Fig. 3 is a schematic cross-sectional view of an element showing one embodiment of a P-channel MOSFET M3 shown in Fig. 1.

Fig. 4 is a constitutional view showing one embodiment of the switching power source according to the present invention.

Fig. 5 is a constitutional view showing another embodiment of the switching power source according to the present invention.

Fig. 6 is a constitutional view showing still another embodiment of the switching power source according to the present invention.

Fig. 7 is a schematic circuit diagram showing another embodiment of the switching power source according to the present invention.

Fig. 8 is a constitutional view showing still another embodiment of the switching power source according to the present invention.

Fig. 9 is a circuit diagram showing one embodiment of a voltage clamping circuit VCL shown in Fig. 8.

Fig. 10 is a circuit diagram showing one embodiment of a level shifting circuit LS2 used in the switching power source

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according to the present invention.

Fig. 11 is a schematic circuit diagram showing still another embodiment of the switching power source according to the present invention.

Fig. 12 is a constitutional view showing still another embodiment of the switching power source according to the present invention.

Fig. 13 is a constitutional view of a step-down type switching power source which is studied prior to the present invention.

Fig. 14 is a view showing operational waveforms of respective parts of the step-down type switching power source shown in Fig. 13.

Explanation of symbols

[0054]

D1 to D4: diode, M1 to M3, M3': MOSFET, Io: current source, Ci: capacitor, CONT: control circuit, EA: error amplifier, CMP: voltage comparator, TWG: triangular wave generating circuit, IB: input circuit, CB: bootstrap capacity, LO: inductor, CO: capacitor, R1 to R4: resistance, INV1 to INV4: CMOS inverter circuit, Reg: power source circuit, LS1, 2: level shifting circuit